AMENDMENTS TO THE SPECIFICATION

Page 1:

In the title, please replace the original title with the following amended title:

Low-Power Semiconductor Memory Device

After the title, please replace the previously inserted paragraph with the following amended paragraph:

CROSS-REFERENCE TO RELATED APPLICATION

This application is a division of Application No. 10/274,985 filed October 22, 2002 (now U.S. Patent No. 6,657,911 issued December 2, 2003).

Page 29:

Please replace the paragraph beginning at line 6 with the following amended paragraph:

FIG. 21 shows a first modification in which the SRAM circuit of FIG. 1 is divided into blocks. In FIG. 21 [[24]], the CHIP as the consolidated LSI includes the logic circuit LOGIC; static memory circuits SRAM1 and SRAM2; an nMOS transistor N9 as a switch between the power source Vss and the ground voltage line Vss1 of the logic circuit; an nMOS transistor N10 as a switch between the power source Vss and a ground voltage line Vssm1 of the SRAM1; the control circuit CNTS outputting the signal cntn controlling the N9 and the N10; and the substrate bias control circuit VBBC

producing the substrate bias Vbn and Vbp. The SRAM circuits SRAM1 and SRAM2 can be of the same construction as that of FIG. 7 and the already described modification of FIG. 7.